REMARKS

Claims 1-25 are pending in the application. Claims 1-25 were rejected. Applicants gratefully acknowledge Examiner's indication that claims 9-25 comprise allowable subject matter and would be allowable if such claims were rewritten in independent form to include their respective base claims and to overcome the rejection of such base claims under 35 U.S.C. § 112.

In response, Applicants have amended claims 1-7, 9 and 17 in a sincere effort to place the application in condition for allowance. For instance, claims 9 and 17 have been made independent by incorporating the elements of their base claim 6. A marked-up version illustrating the claim amendments is annexed hereto. The Examiner's reconsideration of the claim rejections and objections, as well as the specification objections, is respectfully requested in view of the following remarks.

Specification Objection:

An objection was made to the title of the invention as being neither precise nor descriptive. Applicants have amended the title as requested. A marked-up version illustrating the changes to the title of the invention is annexed hereto. Accordingly, the withdrawal of this objection is respectfully requested.

Claim Objection:

An objection was made to claim 7 based on a typographical error. In response, claim 7 has been amended to correct such error. Accordingly, the withdrawal of this objection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 112

Claims 2-25 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly containing subject matter that was not described in the specification regarding "how content of a single stack pointer can insert a one-word item and remove a two-word item from the stack" or "how content of a main stack pointer can insert a one word item and remove a two word item from the stack," as stated in the Office Action. In response to this rejection, notwithstanding that Applicants find nothing in the claims to support this rejection, Applicants respectfully assert that the "content" of a stack pointer does not per se cause a stack operation - - the "content" of a stack pointer is used by, e.g., a digital signal processor, for performing a stack operation such as a "push" or "pop" operation. Indeed, those of ordinary skill in the art are keenly aware of such difference. In any event, the claims as amended are believed to satisfy the requirements of 35 U.S.C. § 112, first paragraph.

Claims 2-25 were also rejected under 35 U.S.C. § 112, first paragraph, as being indefinite. More specifically, with respect to claims 2, 5 and 6, the general phrase "one of A and B" was meant to be synonymous with the phrase "A or B". In any event, the claims as amended are believed to satisfy the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, the withdrawal of all the claims rejections under 35 U.S.C. § 112 is respectfully requested.

Claim Rejections Under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,287,309 to Kai ("Kai") for the reasons set forth on pages 4 and 5 of the Office Action.

Claim 1 is directed to a hardware stack, comprising: a stack storage comprising a plurality of banks each comprising storage locations; and stack pointer circuit comprising a bank pointer for each bank, wherein each bank pointer points to a storage location of a corresponding bank, and wherein the stack pointer circuit is responsive to at least one control signal to insert bank address data in at least two bank pointers to perform a multi-word push or multi-word pop operation.

Although Kai arguably discloses a stack memory 5 comprising a plurality of stack banks 10, 11, it is respectfully submitted that there is nothing in Kai that discloses or suggests the claimed feature of a stack pointer circuit "responsive to at least one control signal to insert bank address data in at least two bank pointers to perform a multi-word push or multi-word pop operation" as recited in claim 1. Indeed, Kai discloses two banks - - one that is dedicated to performing a single-word push operation and another for performing a single-word pop operation (see, e.g., Kai, Col. 3, lines 22-30). The Kai stack memory allows a push and pop operation to be simultaneously commenced using the respective banks so that a stack access operation can be commenced prior to deciding whether the push or pop operation is needed (see, e.g., Col 4, lines 10-20), which effectively increases the access time. Ultimately, however, only one of the single-word stack accesses (e.g., push or pop) is validated (see, e.g., Col. 6, lines 20-32). Thus, there is nothing in Kai that discloses or remotely suggests performing a multi-word push or pop operation as essentially claimed in claim 1.

Furthermore, Kai does not disclose or suggest a stack "bank pointer" associated with each stack "bank", as essentially claimed in claim 1. In contrast, Kai discloses (in Figs. 1 and 2) a single stack pointer (2, 6), which holds an address over all of the stack memory for indicating data to be process by the pop operation (see, e.g., Col. 4, lines 58-60). In short, it is respectfully submitted that Applicants find nothing Kai that discloses or suggests performing "multi-word push" or "multi-word pop" operation, much less a plurality of "bank pointers" that store data for performing such multi-word stack operations, as essentially claimed in claim 1.

Accordingly, claim 1 is believed to be patentably distinct over Kai. Therefore, the withdrawal of the rejections under 35 U.S.C. § 102(b) is respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 2-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kai as applied to claim 1, in view of U.S. Patent No. 6,167,488 to Koppala "(Koppala) for the reasons set forth on pages 5-8 of the Office Action. As explained below, this rejection is legally deficient as neither Kai nor Koppala, alone or in combination, teach or suggest elements of the claimed invention.

Claim 2 is directed to digital data processor that comprises, inter alia, a main stack pointer for pointing to a top location of the stack storage, a plurality of bank pointers, wherein each bank pointer points to a storage location of a corresponding bank based on the content of the main stack pointer; and controller that is responsive to a decoding signal for inserting bank

address data into at least two bank pointers to perform a multi-word push or multi-word pop operation.

Furthermore, independent claim 6 is directed to a digital data processor comprising, *inter alia*, a stack storage comprising a first bank and a second bank; a main stack pointer for pointing to a top location of the stack storage; a first bank stack pointer for pointing to a location assigned to the first bank; a second bank stack pointer for pointing to a location assigned to the second bank; and a stack pointer control logic circuit for controlling the first and second bank stack pointers in response to a decoding signal to insert bank address data into the first and second bank stack pointers based on the content of the main stack pointer to perform a multi-word push or multi-word pop operation

It is respectfully submitted that, at a minimum, the combination of Kai and Koppala is legally deficient as a basis for the rejection of independent claims 2 and 6. In particular, with respect to claims 2 and 6, the combination of Kai and Koppala does not disclose or suggest, for example, performing multi-word stack operations using a plurality of bank pointers that store address data for corresponding banks in the stack, as essentially claimed.

Indeed, as explained above with respect to claim 1, Kai neither discloses nor suggests performing a multi-word push or pop stack operation, much less a plurality of bank pointers for storing address data for corresponding banks in the stack.

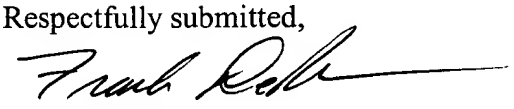
Furthermore, it is respectfully submitted that Koppala does not cure the deficiencies of Kai. Indeed, although Koppala arguably discloses performing multi-word stack operations (see,

Col. 24, lines 27-40), there is nothing in Koppala that discloses or suggests dividing a stack memory into a plurality of banks, much less a separate bank pointer for each bank in the stack that stores address data that is used to perform a multi-word stack operation, as essentially claimed in claims 2 and 6. Therefore, it is respectfully submitted that the combination of Kai and Koppala fails to disclose or suggest performing multi-word stack operations using a plurality of bank pointers that store address data for corresponding banks in the stack, as essentially claimed in claims 2 and 6. Accordingly, claims 2 and 6 are believed to be patentable and non-obvious over the combination of Kai and Koppala.

Moreover, claims 3-5 depend from claim 2 and claims 7-8 depend from claim 6. As such, these claims are believed to be patentably distinct and non-obvious over Kai and/or Koppala for at least the reasons given above for claims 2 and 6. Accordingly, the withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Early and favorable consideration by the Examiner is respectfully urged. Should the Examiner believe that a telephone or personal interview may facilitate resolution of any remaining matters, it is requested that the Examiner contact Applicants' undersigned attorney.

Respectfully submitted,



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MARKED-UP VERSION ILLUSTRATING AMENDMENTS

IN THE SPECIFICATION:

As illustrated in Fig. 1, five items are placed in the 32-word stack 10: A, B, C, D, and E in the order shown. With item E on top of the stack, the content of the stack pointer 20 is 5 (i.e., '00101' in binary). To insert a new item, the stack storage 10 is "pushed" by storing the new item into the location indicated by the stack pointer 20 (i.e., the location at address '5') and then incrementing the stack pointer 20 so as to point to the next-higher order location at address '6'. For removal of the top item E at address '4', the stack storage 10 is "popped" by decrementing the content of the stack pointer 20 first and then retrieving the top item E from the location at address '4', so that the stack pointer 2[1]0 contains '4' to indicate the top location.

Please replace the title of the invention with the following:

APPARATUS FOR CONTROLLING MULTI-WORD STACK OPERATIONS USING A MULTI-BANK STACK IN DIGITAL DATA PROCESSORS

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A hardware stack, comprising:

[an instruction decoder generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a plurality of stack operations;]

a stack storage comprising a plurality of banks each comprising storage locations[, each of the plurality of storage location being classified into one of at least two banks]; and

a stack pointer circuit comprising a bank pointer for each bank, wherein each bank pointer points to a storage location of a corresponding bank, and wherein the stack pointer circuit is responsive to at least one control signal to insert bank address data in at least two bank pointers to perform a multi-word push or multi-word pop operation. [for pointing to at least one of the stack banks of the stack storage in response to at least one decoding signal to thereby cause a stack operation.]

2. (Amended) A digital data processor, comprising:

an instruction decoder for decoding an instruction and generating a plurality of decoding signals;

a stack storage comprising a plurality of banks each comprising storage locations for storing stack items;

a plurality of stack pointers, the stack pointers comprising a main stack pointer for pointing to a top location of the stack storage and a bank pointer for each bank, wherein each bank pointer points to a storage location of a corresponding bank based on the content of the main stack pointer [for pointing to at least one of the locations of said stack storage]; and

a controller responsive to at least one of the decoding signals for inserting bank address data into at least two bank pointers to perform a multi-word push or multi-word pop operation. [stack storage control circuit responsive to the decoding signals, for one of inserting a one-word item into said stack storage and removing a two-word item from said stack storage, based on a content of said stack pointer.]

3. (Amended) The digital data processor of claim 2, wherein each location [of said stack storage] is configured for storing a one-word item.

4. (Amended) The digital data processor of claim 3, wherein a two-word item is one of inserted into and removed from two adjacent locations [of said stack storage] at a given time.

5. (Amended) The digital data processor of claim 4, wherein said [stack storage control circuit] controller either [one of] increases [and] or decreases the content of said main stack pointer by one when the decoding signals indicate a one-word stack operation; and wherein said [stack storage control circuit one of] controller either increases [and] or decreases the content of said main stack pointer by two when the decoding signals indicate a two-word stack operation.

6. (Amended) A digital data processor, comprising:

a stack storage including a plurality of locations, wherein each of the locations of said stack storage are assigned to one of a first bank and a second bank;

a main stack pointer for pointing to a top location of said stack storage;

a first bank stack pointer for pointing to a location assigned to said first bank;

a second bank stack pointer for pointing to a location assigned to said second bank;

an instruction decoder for decoding a stack-based instruction and generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a one-word push operation, a one-word pop operation, a two-word push operation and a two-word pop operation; and

a stack pointer control logic circuit for controlling said first and second bank stack pointers in response to at least one of the decoding signals to insert bank address data into the first and second bank stack pointers based on the content of the main stack pointer to perform a multi-word push or multi-word pop operation [such that at least one of a one-word item and a two-word item is one of inserted into and removed from said stack storage based on a content of said main stack pointer].

7. (Amended) The digital data processor of claim 6, wherein said stack storage comprises 2^{n+1} locations, n being a positive integer, and wherein the first [band] bank and the second bank each include 2^n locations.

9. (Amended) [The digital data processor of claim 6,] A digital data processor, comprising:

a stack storage including a plurality of locations, wherein each of the locations of said stack storage are assigned to one of a first bank and a second bank;

a main stack pointer for pointing to a top location of said stack storage;

a first bank stack pointer for pointing to a location assigned to said first bank;

a second bank stack pointer for pointing to a location assigned to said second bank;

an instruction decoder for decoding a stack-based instruction and generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a one-word push operation, a one-word pop operation, a two-word push operation and a two-word pop operation; and

a stack pointer control logic circuit for controlling said first and second bank stack pointers in response to at least one of the decoding signals to insert bank address data into the first and second bank stack pointers based on the content of the main stack pointer to perform a multi-word push or multi-word pop operation, wherein said stack pointer control logic circuit includes:

an adder for adding one of plurality of predetermined integers to a content of said main stack pointer in response to a first decoding signal from said instruction decoder;

a first selector for selecting for output one of the content of the main stack pointer and a content of said adder in response to a second decoding signal from said instruction decoder, wherein the output of said first selector comprises a high-order bit portion and a low-order bit portion;

a first control logic for generating a first control signal in response to the low-order bit portion of the output from said first selector and a third decoding signal from said instruction decoder;

a second control logic for generating a second control signal in response to the low-order bit portion of the output from said first selector and a fourth decoding signal from said instruction decoder;

an increment logic for incrementing the high-order bit portion of the output from said first selector;

a second selector for selecting one of the high-order bit portion of the output from said first selector and the output of said increment logic in response to the first control signal; and

a third selector for selecting one of the high-order bit portion of the output from said first selector and the output of said increment logic in response to the second control signal;

wherein the outputs of said second and third selectors are provided to said second and first bank stack pointers, respectively.

17. (Amended) [The digital data processor of claim 6,] A digital data processor, comprising:

a stack storage including a plurality of locations, wherein each of the locations of said stack storage are assigned to one of a first bank and a second bank;

a main stack pointer for pointing to a top location of said stack storage;

a first bank stack pointer for pointing to a location assigned to said first bank;

a second bank stack pointer for pointing to a location assigned to said second bank;

an instruction decoder for decoding a stack-based instruction and generating a plurality of decoding signals, each of the plurality of decoding signals denoting one of a one-word push operation, a one-word pop operation, a two-word push operation and a two-word pop operation; and

a stack pointer control logic circuit for controlling said first and second bank stack pointers in response to at least one of the decoding signals to insert bank address data into the first and second bank stack pointers based on the content of the main stack pointer to perform a multi-word push or multi-word pop operation, wherein said stack pointer control logic circuit comprises:

an adder adds one of a plurality of predetermined integers to a high-order bit portion of a content of said main stack pointer in response to a first decoding signal from said instruction decoder;

a control logic for generating one of a first, second, third, and fourth control signals, and combination thereof, in response to a low-order bit portion of the content of said main stack pointer and a second decoding signal from said instruction decoder;

a first selector for selecting one of the high-order bit portion of the content of said main stack pointer and an output of said adder in response to the first control signal;

a second selector for selecting one of the high-order bit portion of the content of said main stack pointer and the output of said adder in response to the second control signal; and

a third selector for selecting one of the high-order bit portion of the content of said main stack pointer and the output of said adder in response to the third control signal;

wherein outputs of said second and third selector are provided to said second and first bank stack pointers, respectively, and the low-order bit portion of the content of said main stack pointer is controlled by the fourth control signal.